SBC-85 Bus Monitor Supreme

This user's guide describes the SBC-85 Bus Monitor Supreme

Notation:

Pin numbers. Pin numbers are given as ***ID.pin***. for example, Pin 5 of connector X3 is given as ***X3.5***. IC7 pin 21 is given as ***IC7.21***.

Logic Levels. Lines having a signal that is active low is given with either an asterisk or a slash following the signal name. For example, **CS8/** and **CS11*** both refer to signals that is active when at 0V or logic low.

Terminology:

Most abbreviations will be spelled out when they are first used. However, the more commonly used terms are described in the ***Definitions of Terms and Notations*** at the end of the document.

The term ***stop-for-step*** is a key term used as a reference to any one of several trigger events that stops the CPU. The CPU is restarted by one of a few mechanisms that clear the stop-for-step mode and put the CPU back into run mode.

SBC-85 BUS MONITOR DESCRIPTION

The SBC-85 bus monitor is a part of the 8085 based Single Board Computer System. The bus monitor provides a binary display of the values 16-bit address values and 8-bit data on the backplane. In addition to the binary display, these values are decoded as eight nibbles, converted to hexadecimal, and displayed on six 7-segment LED displays. The board includes program single step based on the specific type of bus cycle (e.g., memory read, I/O write, opcode fetch, etc.) as well as an automatic "slow-step" which advances through the code at a user controlled rate from approximately 0.5 Hz to 60 Hz. Through the use of four I/O registers, the user can load address and/or data breakpoints to the bus monitor. When the breakpoint is matched during program execution, the bus monitor will stop the program until the single step button is pushed or the slow-step automatically advances past the breakpoint.

COMPONENT OVERVIEW

Primary

U1, U2, U3, U4, U5 – 74LS541 buffers to drive data from the edge connector to onboard components

U10, U11, U12, U13, U14, U15 – MC14495P1 4-bit binary to hexadecimal decoder/drivers with six common cathode 7-segment LED displays.

SW2 – 10-position BCD coded rotary switch to select the type of bus cycle that triggers a stop-for-step.

U27, RV1 – a 555 timer running in astable mode to generate a continuous pulse train to trigger the automatic slow-step

SW3 – a momentary single-step push button that clears the stop-for-step mode.

SW1 – a 6 position DIP switch to set the most significant bits of the four onboard port address for the command register, two address breakpoint registers, and data breakpoint register.

U16 – an 8-bit equality detector to enable the onboard command and data registers.

U18, U19, U20, U21 – 8-bit latches serving as, respectively, the command register, Address LSB breakpoint register, address MSB breakpoint register, and data breakpoint register.

U22, U23, U24 – 8-bit comparators to trigger a breakpoint stop-for-step when the address and/or data match the values in their respective register.

Glue

U7 – 74LS139 dual 2-to-4 decoder. U7A used to identify and generate an Opcode Fetch interrupt, U7B used to decode the port output address to select the command register or data register.

U8 – 74LS08 Quad 2-input AND gate. U8A gates the 555 pulse train based on the position of SW4 to create the SlowStep* signal. U8B gates the data breakpoint to be latched only during an I/O read or write. U8C gates the command register StepEnable signal to override the single step mode and force the CPU into a run condition. U8D unused.

U9 – 74LS74 dual D-type latch. U9A is used to latch the stop-for-step upon a data breakpoint match. U9B is used to one-shot the single-step-advance signal which clears the stop-for-step signal and restores the CPU ready signal.

U25 – Quad 2-input AND gate. U25A creates a logic TRUE when both the MSB and LSB of the bus address match the MSB and LSB address in the registers. U25B gates the full address match breakpoint with bit4 of the command register to enable or disable the full address match breakpoint. U25C gates the MSB OR LSB address match breakpoint with bit5 of the command register to enable or disable the either MSB or LSB address match breakpoint. U25D gates the data match signal with bit6 of the command register to enable or disable the data breakpoint.

U26 – 74LS32 Quad 2-input OR gate. U26A creates a logic TRUE when either the MSB OR the LSB of the bus address match their respective address register. U26B creates a logic TRUE when the net result of all other matching and gating results in n address breakpoint match. U26C creates a STEP_Condition_TRUE signal when either the rotary bus state mode selector is set to ANY (i.e., Always Arm) or the Address breakpoint is matched. U26D sets the D-input to U32A when either the MachineStateMatch signal or the STEP_Condition_TRUE signal is set.

U28 – 74138 1-of-8 decoder to illuminate a LED indicating which filter is being applied to the bus cycle stop-for-step.

U30 – 74LS85 4-bit comparator used to match the target bus cycle type to trigger a stop-for-step.

U31 – 74LS00 Quad 2-input NAND gate. U31A and U31B debounce the manual STEP button. U31C uses the bus RD* and WR* signals to create a RD or WR signal. U31D is used to trigger a stop-for-step reset signal whenever the manual STEP push button is pressed OR when a SlowStep pulse is received.

U32 – 74LS74 dual D-type latch. U32A is used to latch the stop-for-step upon a matching machine state or matching address breakpoint condition. U32B is used as the main RS flip-flop to place the CPU in a wait state or run state by controlling the READY line.

U33 – 74LS01 open collector quad 2-input NAND used to pull down the READY signal to the CPU when the system is in a stop-for-step state.

CIRCUIT DESCRIPTION

BUS BUFFER

To prevent significant loading of the bus, all signals are buffered using 74LS541 octal Schmitt trigger buffers U1, U2, U3, U4, U5. The buffered signal is given the same name as the incoming signal with the prefix ***b*** for buffered, e.g., CLK becomes bCLK. While the'541 has 3-state outputs, the outputs are wired to be continuously enabled. Each output of the '541 can sink 30 mA and source 18mA which is sufficient to sink the low current common anode LEDs or source the common cathode LEDs as well as drive the hex decoders and remaining devices.

ADDRESS AND DATA DISPLAY

The 74LS541 is used as the primary driver for individual 1mA LED configured with a resistor pack to ground. Since the builder may choose different colored LEDs for each nibble, the 4-resistor networks allow values to be selected to adjust the perceived brightness of that LED color. Each nibble of the address and display is also presented to a Motorola MC14495P1 binary to hex decoder and display driver. These drivers are internally current limited so they merely need to be connected to a common cathode 7-segment display.

Command Register, Breakpoint Registers

The bus monitor occupies four port addresses with a base address set by DIP switch SW1. SW1.1 – SW1.6 determines the six most significant bits of the base port address for the onboard registers. Open switch to match address = 1, close switch to match address =0. SW1.1 is the most significant address. For example, SW1.1 – SW1.6 Open, Open, Open, Open, Close, Close = port address 0xF0-0xF3.

All registers are write only and cannot be read back, they are standard 8-bit, I/O mapped, ports with the following addresses:

- Command Register = Base Address
- Address Breakpoint LSB Register = Base Address +1
- Address Breakpoint MSB Register = Base Address +2
- Data Breakpoint Register = Base Address +3

Command Register. Base Address

The individual bits of the command register control the following:

Bit	**Function**	**Set**	**Reset**
0 (LSBit)	Step Enable	Enable Step	Force *RUN* mode
1	S0 condition	Match S0=1	Match S0=0
2	S1 condition	Match S1=1	Match S1=0
3	IO.M* condition	Match IO/M* = 1	Match IO/M* = 0
4	Full Address Match	Enable Full Address Match	Disable Full Address Match
5	Bytewise Address Match	Match MSB OR LSB	Disable Bytewise Match
6	Data Breakpoint	Enable Data Byte Match	Disable Data Byte Match
7 (MSBit)	Speaker	Toggle for tone	

Note that the speaker is pulled down to energize, i.e., bit 7 = 0 (reset) energizes the speaker and bit 7 =1 (set) de-energizes the speaker. Useful knowledge if you are replacing the speaker with something else.

Address Least Significant Byte Register. Base Address+1

The 8-bit Address LSB register is loaded by the software to the target most significant byte address (A15-A8) which will generate a stop-for-step trigger.

Address Most Significant Byte Register. Base Address+1

The 8-bit Address MSB register is loaded by the software to the target most significant byte address (A7-A0) which will generate a stop-for-step trigger.

Data Byte Register. Base Address+1

The 8-bit Address Data register is loaded by the software to the target data byte pattern which will generate a stop-for-step trigger.

SINGLE STEP

Single stepping is accomplished by taking the 8085 READY input line low which places the CPU into a wait state until the READY is returned high. This is intended to be an open collector signal with a pullup on the SBC-85 board, so all other devices must connect to this signal with an open collector device. On the Bus Monitor Supreme board, single step is accomplished through one of several mechanisms that put the monitor in a stop-for-step mode which places the CPU in the wait state. To exit the wait state, another mechanism must clear this mode so the program can continue until the next stop-for-step condition is met.

IMPORTANT NOTE: Stop-for-Step triggers are ORed, i.e., if both a bus cycle type filter is set and an address breakpoint is set the system will trigger a stop-for-step when either condition occurs.

For any step mode to be enabled, SW4 must be in either the center or down position. When SW4 is in the up position, U8.10 is FALSE so the output of U8C is FALSE and the second input to U33A is immaterial.

The single step portion of the bus monitor circuit description will be sub-divided into four portions:

- Bus cycle type filter;
- Breakpoint trigger;
- Step set; and,
- Step clear.

Bus Cycle Type Filter

At the beginning of each bus cycle the 8085 outputs its status signals IO/M*, S1, and S0. These signals can be decoded to determine what type of bus cycle is about to occur. The bus monitor compares these three status lines with the pattern for the desired type of bus cycle and if they match a stop-for-step signal is triggered. The decoding of the status lines is as follows:

8085 Bus Cycle Status Signals			
IO/M*	**S1**	**S0**	**Cycle Type**
0	0	0	N/A
0	0	1	Memory Write
0	1	0	Memory Read
0	1	1	Opcode Fetch

1	0	0	N/A
1	0	1	I/O Write
1	1	0	I/O Read (or DAD)
1	1	1	Interrupt Acknowledge

The user has two means of selecting which cycle filter is selected. If Jumpers are placed between posts 2 and 3 on JP7, JP8, and JP9, the onboard rotary switch is used to select which filter is used. Any that have a jumper between posts 1&2 the corresponding bit of the command register is matched rather than the switch position.

The switch filter selection consists of a 10-position BCD complement output rotary encoded switch with its common to 0V and pull up resistors on each of its four outputs. These outputs are tied to pin 3 of the three selection jumpers JP7, JP8, and JP9 mentioned previously. With switch positions 0-7 the rotary switch directly creates the bit patten for IO/M*, S1, and S0. In switch positions 8 and 9 the filter is disabled and any bus cycle will trigger a stop-for-step.

The three match bits, either created by the BCD switch or the command register, are decoded using a 3-to-8 decoder whose output sinks one of eight LEDs indicating which filter is selected. In positions 8 or 9 the filter is OFF meaning any bus cycle will trigger the stop-for-step so all LEDs are turned off by disabling the 1-of-8 decoder. The match bits are also compared against the 8085 values bIO/M*, bS1, and bS0 using the four-bit comparator U30 74LS85. The A=B output goes high when the actual machine state matches the specified machine state.

The first net result of the bus cycle type filter is the MachineStateMatch signal which goes TRUE when the bus cycle type matches the filter. The second net result is the AlwaysArmStep which goes TRUE when the bus cycle type filter is disabled.

Breakpoint Trigger

There are three breakpoint triggers: Address MSB, Address LSB, and Data Byte. The values for these are individually loaded into their respective registers, i.e., ports Base+1, Base+2, and Base+3 which latch into U19, U20, and U21 respectively. The address or data bits in these registers are compared to their corresponding address or data bit on the bus via individual 8-bit comparators for each byte. The comparators have two outputs: Equal* and Greater*, either of which can be selected via jumpers JP3, JP4, and JP5. These outputs are inverted to create their corresponding Equal or Greater signal (Greater means the bus address (data) is greater than the corresponding register value). The MSB and LSB of the address are then logically ANDed or ORd to create one signal if the entire address matches and a second signal if either the high or low byte match. These two signals are then gated with bit 4 and 5 from the command register, i.e., they are enabled if the corresponding bit is TRUE and the breakpoint signal is disabled if the command bit is FALSE. Likewise for the data byte which is gated with bit 6 of the command register to enable or disable the data match breakpoint.

The net result of the breakpoint are the AddressBreakPointMatch signal and the DataBreakPointMatch. These remain as separate signals because they must be synchronized differently.

Step Set

To this point the bus type filter and breakpoint matching has completely ignored any timing, i.e., changing signals, bus transitions, and noise is allowed to propagate with reckless abandon through the entire comparator and logic system. This all stops at the Step Set latches where the signals are synchronized with the bus state to exclude transient states.

The DataBreakpointMatch signal is hardware enabled with JP11, 1-2 to enable, 2-3 to disable. This signal is only valid during a bus read or write cycle and only on the falling edge of the 8085 CLK because the data bus, at times, has the low 8 bits of the address or may have a port address. This timing is accomplished by a logical AND of the breakpoint match signal with the RD or WR signal to create the D-input to the latch. Therefore, IF a data match breakpoint is true AND it is a RD or WR cycle, a logic TRUE is latched during the rising edge of bCLK*. If the data breakpoint is not matched or if it is not a RD or WR cycle, then a logic FALSE is latched. The Q* output of this latch is a DataBreakPointMatchPending* signal which indicates at some time in the past the bus data matched the data in the data register. This signal asynchronously sets the Q output of latch U32A to enable the STEP_Mode* signal.

The bus type and AddressBreakpointMatch signals are also completely asynchronous with the bus cycle and must be latched at the proper time. For both of these, that time is the falling edge of the 8085 Address Latch Enable (ALE), a.k.a., the rising edge of bALE. Therefore, the bus cycle type matches the filter, OR if the address breakpoint is TRUE, OR if the BCD switch is set to ANY bus state, when the bALE* rises that TRUE signal is latched into U32A and its inverted output Q* creates a STEP_Mode* signal.

Once U32A activates the STEP_Mode* (either directly from the D input or indirectly from the S* input from the databreakpoint) the InStep RS flip-flop U32B is reset, its Q* output goes high which is then inverted by U33A taking the READY line low (presuming that RUN* is TRUE).

Step Clear

As described above, the stop-on-step can be triggered by the address match, data match, bus cycle type filter, or any bus cycle. All of these place the RS flip-flop U32B into the “InStep” mode which then pulls the READY line low if the signal is gated with a disabled RUN signal. A reset of the InStep is a matter of providing a reset to the D-latches U9A, U32A and for the RS latch U32B. This reset is generated as follows:

An active low pulse is generated either by the 555 astable timer gated by U8A controlled by SW4. The pulse train is allowed through this gate when the switch is in the DOWN position (slow step). This SlowStep* pulse train is logically ORed and inverted (by U31D NAND gate) with a manually generated pulse ManualStep* generated by SW5 or offboard switch connected to J3 and their corresponding debounce circuit created by U31A and U31B. The resulting positive edge going pulse is used as the CLK input to D-latch U9B whose D-input is the InStep signal. Therefore, whenever the pulse train or the manual switch generates a step signal (a.k.a., exit wait state), the Q* output of this latch goes low to create an ExitSTEP* signal. This low going signal is connected to the Reset* inputs of the two D-latches U9A and U32A and to the Set* input of the final RS latch. This ExitStep* signal is also connected to the Reset* input of its own latch, thereby clearing itself after a short pulse. Obviously, by definition this short pulse will Reset itself, but it will reliably Set or Reset the other latches. Nonetheless, the pulse length is stretched with the use of the RC C47 where the *R* component is provided by the pull ups in the latches.

EXPANSION BUS

The mating card edge connector is a 120 pin PCI connector, e.g., TE Connectivity AMP PN 5145167-8.

Expansion bus signals are shown by the following table:

Expansion Bus Pinout							
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	Ground	31	R31	61	+5V	91	R91
2	Ground	32	R32	62	+5V	92	R92

3	Ground	33	R33	63	+5V	93	R93
4	Ground	34	READY	64	+5V	94	R94
5	Ground	35	CLK	65	+5V	95	R95
6	A8	36	HLDA	66	AD7	96	R96
7	A9	36	HOLD	67	AD6	97	R97
8	A10	38	ALE*	68	AD5	98	R98
9	A11	39	R39	69	AD4	99	R99
10	A12	40	R40	70	AD3	100	R100
11	A13	41	R41	71	AD2	101	R101
12	A14	42	R42	72	AD1	102	R102
13	A15	43	R43	73	AD0	103	R103
14	A0	44	R44	74	INTA*	104	R104
15	A1	45	R45	75	S0	105	R105
16	A2	46	R46	76	INTR	106	R106
17	A3	47	R47	77	ALE	107	R107
18	A4	48	R48	78	RST 5.5	108	R108
19	A5	49	R49	79	WR*	109	R109
20	A6	50	R50	80	RST 6.5	110	R110
21	A7	51	R51	81	RD*	111	R111
22	R22	52	R52	82	RST 7.5	112	R112
23	R23	53	R53	83	S1	113	R113
24	R24	54	R54	84	TRAP	114	R114
25	R25	55	R55	85	IO/M*	115	R115
26	R26	56	Ground	86	SID	116	+5V
27	R27	57	Ground	87	SOD	117	+5V
28	R28	58	Ground	88	R88	118	+5V
29	R29	59	Ground	89	R89	119	+5V
30	R30	60	Ground	90	R90	120	+5V
Note: All “R” signals are reserved for user							

COMPONENTS

UNUSED GATES

U6E 74LS04 Hex Inverter

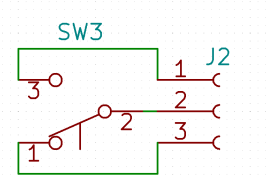
U33B, U33C, U33D 74LS01 Quad 2-Input NAND Open Collector Output

CONNECTORS

J1 Expansion Bus. 120 PCI connector (physical format only)

J2 External Single Step Switch

An external single step can be connected. If the switch is not used, pins 1-2 must be jumpered on the bus monitor board. If the switch is used, it should be SPDT momentary, i.e., ON-NONE-(ON).



JUMPERS

JP1 Selects a hardware interrupt when an AddressBreakpointMatch becomes true. 2 is the signal, pin 1-RST7.5, 3-TRAP, 4-RST5.5, 5- RST6.5.

JP2 Selects a hardware interrupt for an opcode fetch. Pin 2 is the signal, pin1-RST7.5, 3-TRAP, 4-RST5.5, 5- RST6.5.

JP3 Selects if LSB of Address is matched by equality or if the bus address is greater than the Command Register value. 1-2 Equal, 2-3 bus address > register address. Useful if the user wants to trigger a stop-for-step whenever the address exceeds a given value, e.g., when the program counter is greater than any threshold LSB address byte.

JP4 Selects if MSB of Address is matched by equality or if the bus address is greater than the Command Register value. 1-2 Equal, 2-3 bus address > register address. Useful if the user wants to trigger a stop-for-step whenever the address exceeds a given value, e.g., when the program counter is greater than any threshold MSB address byte.

JP5 Selects if Data is matched by equality or if the bus data is greater than the Command Register value. 1-2 Equal, 2-3 bus data > register data. Useful if the user wants to trigger a stop-for-step whenever the data byte exceeds a specified value.

JP6 Enables the Address Breakpoint stop-to-step trigger. 1-2 Enabled, 2-3 Disabled

JP7 Selects between BCD rotary switch (SW2) and command register for the bus cycle match of S0. 1-2 is command register control Bit 1, 2-3 is SW2 control.

JP8 Selects between BCD rotary switch (SW2) and command register for the bus cycle match of IO/M*.1-2 is command register control Bit 3, 2-3 is SW2 control.

JP9 Selects between BCD rotary switch (SW2) and command register for the bus cycle match of S1. 1-2 is command register control Bit 2, 2-3 is SW2 control.

JP10 Enables or disables software override of single step. 1-2 Command Status Bit 0 controls step enable (1=enable step, 2=Run); 2-3 Step Enabled.

JP11 Enables the Data Breakpoint trigger for stop-for-step. 1-2 Enable data breakpoint, 2-3 Disable data breakpoint.

JP12 Enables or Disables pull down of the bus READY line, thereby controlling if the bus monitor board can put the CPU in a wait state for single step. *Inserted* Enable Step Mode, *Removed* Disable all step modes.

LEDs (alphabetical by silkscreen)

A1 (AFF4) 7-segment Low Nibble of Least significant address Byte

A2 (AFF3) 7-segment High Nibble of Least significant address Byte

A3 (AFF2) 7-segment Low Nibble of Most significant address Byte

A4 (AFF1) 7-segment High Nibble of Most significant address Byte

D1 (AFF6) 7-segment Low Nibble of Data Byte

D2 (AFF5) 7-segment High Nibble of Data Byte

ALE (D5) ON = Address Latch Enable Active (low)

ANY (D53) ON = Stop-For-Step Filter set for ANY bus cycle.

CLK (D10) ON = CLK active (high)

HLDA (D19) ON = Hold Acknowledge active (high)

HOLD (D18) ON = HOLD active (high)

INTA (D7) ON = Interrupt Acknowledge signal active (low).

INTA (D52) ON = Bus Cycle filter set to Interrupt Acknowledge.

INTR (D14) ON = Interrupt request is active (high)

IORD (D51) ON = Bus Cycle filter set to IO Read.

*IO/M** ON = Bus cycle type IO, OFF = Bus cycle type is Memory

IOWR (D50) ON = Bus Cycle filter set to IO Write.

MRD (D47) ON = Bus Cycle Filter set to Memory Read.

MWR (D46) ON = Bus Cycle Filter set to Memory Write.

OFF (D45 & D49) ON = Bus Cycle Filter turned off, i.e., will not trigger stop-for-step.

OpFetch (D48) ON = Bus Cycle Filter set to Opcode Fetch.

RD (D3) Read Signal active (low).

READY (D20) ON = READY signal active (high)

RST 5.5 (D15) ON = RST 5.5 signal active (high)

RST 6.5 (D16) ON = RST 5.5 signal active (high)

RST 7.5 (D17) ON = RST 5.5 signal active (high)

RUN (D54) ON = Stop-on-Step is off so CPU READY line is left alone. “ON” either because SW4 is in the up (RUN) position or JP10 is set to 1-2 and Control Register Bit 0 is set to 0.

S0 (D12) Status Signal S0 active (high)

S1 (D13) Status Signal S1 active (high)

SID (D8) SID signal active (high)

SOD (D9) SOD signal active (high).

STEP (D2) ON = exit step triggered, i.e., either manual push button pressed or pulse train actively clearing the wait state condition to return the CPU to run mode.

TRAP (D5) TRAP interrupt signal active (high)

WR (D4) Write Signal active (low).

RESISTORS

R6 Current limiting for ANY (D53), 330 Ω adjust for desired brightness.

R7 Threshold series resistor for 555 timer, combined with RV1 (or RV2) to set reset threshold voltage

R8 10KΩ pull up for SW4.

R9 10KΩ pull up for SW5

R10 10KΩ pull up for SW5

R11 Current limiting for RUN (D54), 330 Ω adjust for desired brightness.

R12 Pull up for speaker, 330 Ω

R13 Current limiting for STEP (D2), 330 Ω adjust for desired brightness.

R14 Current limiting for StepOverride (D55), 330 Ω adjust for desired brightness.

RN1 7-resistor common rail network, pull-up for D4, D4, D5, D6, D7, D8, D9. 330 Ω -470 Ω or as desired for LED brightness

RN2 7-resistor common rail network, pull-down for D10, D11, D12, D13, D18, D19, D20. 330 Ω -470 Ω or as desired for LED brightness

RN3 4-resistor common rail network, pull-down for D21, D22, D23, D24. 330 Ω -470 Ω or as desired for LED brightness

RN4 4-resistor common rail network, pull-down for D25, D26, D27, D28. 330 Ω -470 Ω or as desired for LED brightness

RN5 4-resistor common rail network, pull-down for D29, D30, D31, D32. 330 Ω -470 Ω or as desired for LED brightness

RN6 4-resistor common rail network, pull-down for D33, D34, D35, D36. 330 Ω -470 Ω or as desired for LED brightness

RN7 4-resistor common rail network, pull-down for D37, D38, D39, D40. 330 Ω -470 Ω or as desired for LED brightness

RN8 4-resistor common rail network, pull-down for D41, D42, D43, D44. 330 Ω -470 Ω or as desired for LED brightness

RN10 4-resistor common rail network, pull-down for D14, D15, D16, D17. 330 Ω -470 Ω or as desired for LED brightness

RV1 200KΩ potentiometer populate one or the other. RV1 footprint 4 turn, RV2 footprint 1 turn

RV2 1 turn alternative to RV1

SWITCHES

SW1 Determines the six most significant bits of the base port address for the onboard registers. Open switch to match address = 1, close switch to match address =0. SW1.1 is the most significant address. For example, SW1.1 – SW1.6 Open, Open, Open, Open, Close, Close = port address 0xF0-0xF3.

SW2 Selects the bus cycle type filter for the stop-for-step trigger according to the following table:

SW2 Stop-for-Step Bus Cycle Filter				
Switch Position	**IO/M***	**S1**	**S0**	**Cycle Type**
0	0	0	0	N/A
1	0	0	1	Memory Write
2	0	1	0	Memory Read
3	0	1	1	Opcode Fetch
4	1	0	0	N/A
5	1	0	1	I/O Write
6	1	1	0	I/O Read (or DAD)
7	1	1	1	Interrupt Acknowledge
8	x	x	x	Any Bus Cycle
9	x	x	x	

SW4 3 position RUN-STEP-SLOW STEP select switch. UP = RUN mode where all stop-for-step triggers are ignored, CENTER = Single Step mode where button SW5 advances out of the current step, DOWN = Slow Step mode where the onboard 555 pulse train automatically advances the step at a rate set by RV1 (or RV2)

SW5 Momentary push button switch which advances the STEP. Push to clear the 8085 wait state and thereby exiting the current step.

REVISIONS

v1.0 First produced board week 0520

1.01 Removed Pulse Train LED and combined with manual step button to create STEP LED. Required swapping U31d with U6E to keep LED primarily off
1.02 Changed Pull-Up BCD switch to complement output take to 0V and changed R2, R3,R4,R5 to pull-up to improve signal levels.
1.03 Reworked ExitStep* reset latch U9B, D-Input as InStep.
1.04 Adjust 7-segment placement
1.05 Add additional decoupling caps in NW corner of board
1.06 Add StepOverride LED
1.07 Corrected transposed bS0 and bIO/M* on U30
1.08

v1.1 Second produced board week 1020

APPLICABLE DATA SHEETS

74LS00 Quad 2-input NAND gate

74LS01 Quad 2-input NAND gate with Open Collector Output

74LS04 HEX inverter

74LS08 Quad 2-input AND gate.

74LS32 Quad 2-input OR gate

74LS74 dual D-type latch.

74LS85 4-bit comparator

74138 1-of-8 decoder

74LS139 dual 2-to-4 decoder.

74LS541 octal buffer with 3-state outputs

74LS573 Octal transparent latch with 3-state Outputs (alternative pinout to ‘373)

74LS373 Octal transparent latch with 3-state Outputs (for details not in ‘573 data sheet)

74LS682 8-bit Magnitude Comparator

MC14495P1 4-bit binary to hexadecimal decoder/drivers

555 timer running in astable mode

LTS-6980HR Common Cathode 7-Segment LED Display

Definitions of Terms and Notation

0xF

Hex Interpretation of 4 binary bits (nibble), in this example HEX F which is 1111 in binary

0xFF

Hex Interpretation of 8 binary bits (byte), in this example HEX FF which is 1111 1111 in binary

0xFFFF

Hex Interpretation of 16 binary bits or Word (two bytes). In this example HEX FFFF is the interpretation of the binary value 1111 1111 1111 1111

A*n*

Individual Address Line where n is 0-15

AD*n*

Individual Multiplexed Address / Data line where n is 0-8

Byte

8-bits

Component Side

The 'top' of the PC board where the components are mounted. On the SBC-85 this is the side with the bulk of the silkscreen and the component numbers and footprints.

CS/ or CS*

Chip Select (reverse, a.k.a., negative logic) where a logic LOW (0v) is active

U*n*

Integrated Circuit ID n

LSB

Least Significant Byte

LSBit

Least Significant Bit

MSB

Most Significant Byte

MSBit

Most Significant Bit

Nibble

4-bits

On

Logic TRUE or active. May be HIGH (+5V) or LOW (0V)

Off

Logic FALSE or inactive. May be HIGH (+5V) or LOW (0V)

SWn

Switch were n is the switch identifier

SID

Serial Input Data (8085 pin 5)

SOD

Serial Output Data (8085 pin 4)

Solder Side

The 'bottom' of the PC board

UART

Universal Asynchronous Receiver Transmitter. A serial port controller that autonomously handles asynchronous serial communication e.g., RS232

USART

Universal Synchronous Asynchronous Receiver Transmitter. A serial port controller that autonomously handles either synchronous or asynchronous serial communication e.g., RS232